AT89C2051 Microcontroller

Instructions

1.1 Features

- Compatible with MCS-51 Products
- 2 Kbytes of Reprogrammable Flash Memory
  Endurance: 1,000 Write/Erase Cycles
- 2.7 V to 6 V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Two-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 15 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial UART Channel
- Direct LED Drive Outputs
- On-Chip Analog Comparator
- Low Power Idle and Power Down Modes

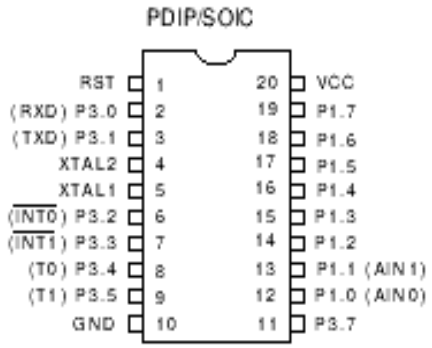
1.2 Description

The AT89C2051 is a low-voltage, high-performance CMOS 8-bit microcomputer with 2 Kbytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51 instruction set and pinout. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C2051 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

The AT89C2051 provides the following standard features: 2 Kbytes of Flash, 128 bytes of RAM, 15 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, a precision analog comparator, on-chip oscillator and clock circuitry. In addition, the AT89C2051 is designed with static logic for

operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

1.3 Pin Configuration



1.4 Pin Description

VCC Supply voltage.

GND Ground.

Port 1

Port 1 is an 8-bit bidirectional I/O port. Port pins P1.2 to P1.7 provide internal pullups. P1.0 and P1.1 require external pullups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. The Port 1 output buffers can sink 20 mA and can drive LED displays directly. When 1s are written to Port 1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs and are externally pulled low, they will source current (IIL) because of the internal pullups.

Port 1 also receives code data during Flash programming and program verification.

Port 3

Port 3 pins P3.0 to P3.5, P3.7 are seven bidirectional I/O pins with internal pullups. P3.6 is hard-wired as an input to the output of the on-chip comparator and is not accessible as a general purpose I/O pin. The Port 3 output buffers can sink 20 mA. When 1s are written to

Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pullups.

Port	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)

Port 3 also serves the functions of various special features of the AT89C2051 as listed below:

1.5 Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divideby-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

1.6 Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in the table below.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses. to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new fea tures. In that case, the reset or inactive values of the new bits will always be 0.

1.7 Restrictions on Certain Instructions

The AT89C2051 and is an economical and cost-effective member of Atmel's growing family of microcontrollers. It contains 2 Kbytes of flash program memory. It is fully compatible with the MCS-51 architecture, and can be programmed using the MCS-51 instruction set. However, there are a few considerations one must keep in mind when utilizing certain instructions to program this device.

All the instructions related to jumping or branching should be restricted such that the destination address falls within the physical program memory space of the device, which is 2K for the AT89C2051. This should be the responsibility of the software programmer. For example, LJMP 7E0H would be a valid instruction for the AT89C2051 (with 2K of memory), whereas LJMP 900H would not.

1. Branching instructions:

LCALL, LJMP, ACALL, AJMP, SJMP, JMP @A+DPTR

These unconditional branching instructions will execute correctly as long as the programmer keeps in mind that the destination branching address must fall within the physical boundaries of the program memory size (locations 00H to 7FFH for the 89C2051). Violating the physical space limits may cause unknown program behavior.

CJNE [...], DJNZ [...], JB, JNB, JC, JNC, JBC, JZ, JNZ With these conditional branching instructions the same rule above applies. Again, violating the memory boundaries may cause erratic execution.

For applications involving interrupts the normal interrupt service routine address locations of the 80C51 family architecture have been preserved.

2. MOVX-related instructions, Data Memory:

The AT89C2051 contains 128 bytes of internal data memory. Thus, in the AT89C2051 the stack depth is limited to 128 bytes, the amount of available RAM. External DATA memory access is not supported in this device, nor is external PROGRAM memory execution. Therefore, no MOVX [...] instructions should be included in the program.

A typical 80C51 assembler will still assemble instructions, even if they are written in violation of the restrictions mentioned above. It is the responsibility of the controller user to know the physical features and limitations of the device being used and adjust the instructions used correspondingly.

1.8 Program Memory Lock Bits

On the chip are two lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

Lock Bit Protection Modes(1)

Program Lock Bits			
	LB1	**LB2**	**Protection Type**
1	U	U	No program lock features.
2	P	U	Further programming of the Flash is disabled.
3	P	P	Same as mode 2, also verify is disabled.

Note: 1. The Lock Bits can only be erased with the Chip Erase operation

1.9 Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

P1.0 and P1.1 should be set to '0' if no external pullups are used, or set to '1' if external pullups are used.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

1.10 Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers

retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before VCC is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

P1.0 and P1.1 should be set to '0' if no external pullups are used, or set to '1' if external pullups are used.

1.11 Programming The Flash

The AT89C2051 is shipped with the 2 Kbytes of on-chip PEROM code memory array in the erased state (i.e., contents = FFH) and ready to be programmed. The code memory array is programmed one byte at a time. *Once the array is programmed, to re-program any non-blank byte, the entire memory array needs to be erased electrically.*

Internal Address Counter**:** The AT89C2051 contains an internal PEROM address counter which is always reset to 000H on the rising edge of RST and is advanced by applying a positive going pulse to pin XTAL1.

Programming Algorithm**:** To program the AT89C2051, the following sequence is recommended.

1. Power-up sequence:

Apply power between VCC and GND pins Set RST and XTAL1 to GND

With all other pins floating, wait for greater than 10 milliseconds

2. Set pin RST to 'H' Set pin P3.2 to 'H'

3. Apply the appropriate combination of 'H' or 'L' logic levels to pins P3.3, P3.4, P3.5, P3.7 to select one of the programming operations shown in the PEROM Programming Modes table.

To Program and Verify the Array:

4. Apply data for Code byte at location 000H to P1.0 to P1.7. 5. Raise RST to 12V to enable programming.

6. Pulse P3.2 once to program a byte in the PEROM array or the lock bits. The byte-write cycle is self-timed and typically takes 1.2 ms.

7. To verify the programmed data, lower RST from 12V to logic 'H' level and set pins P3.3 to P3.7 to the appropiate levels. Output data can be read at the port P1 pins.

8. To program a byte at the next address location, pulse XTAL1 pin once to advance the internal address counter. Apply new data to the port P1 pins.

9. Repeat steps 5 through 8, changing data and advancing the address counter for the entire 2 Kbytes array or until the end of the object file is reached.

10. Power-off sequence: set XTAL1 to 'L' set RST to 'L'

Float all other I/O pins Turn Vcc power off

Data Polling: The AT89C2051 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P1.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The Progress of byte programming can also be monitored by the RDY/BSY output signal. Pin P3.1 is pulled low after P3.2 goes High during programming to indicate BUSY. P3.1 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed code data can be read back via the data lines for verification:

1. Reset the internal address counter to 000H by bringing RST from 'L' to 'H'.

2. Apply the appropriate control signals for Read Code data and read the output data at the port P1 pins.

3. Pulse pin XTAL1 once to advance the internal address counter.

4. Read the next code data byte at the port P1 pins. 5. Repeat steps 3 and 4 until the entire array is read.

The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire PEROM array (2 Kbytes) and the two Lock Bits are erased electrically by using the proper combination of control signals and by holding P3.2 low for 10 ms. The code array is written with all "1"s in the Chip Erase operation and must be executed before any non-blank memory byte can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 001H, and 002H, except that P3.5 and P3.7 must be

pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel (001H) = 21H indicates 89C2051

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Ultrasonic ranging system design

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ABSTRACT：Ultrasonic ranging technology has wide using worth in many fields，such as the industrial locale，vehicle navigation and sonar engineering．Now it has been used in level measurement，self-guided autonomous vehicles, fieldwork robots automotive navigation，air and underwater target detection，identification，location and so on．So there is an important practicing meaning to learn the ranging theory and ways deeply. To improve the precision of the ultrasonic ranging system in hand，satisfy the request of the engineering personnel for the ranging precision，the bound and the usage，a portable ultrasonic ranging system based on the single chip processor was developed．

Keywords：Ultrasound r，Ranging System，Single Chip Processor

1.Introductive

With the development of science and technology, the improvement of people's standard of living, speeding up the development and construction of the city. urban drainage system have greatly developed their situation is constantly improving. However, due to historical reasons many unpredictable factors in the synthesis of her time, the city drainage system. In particular drainage system often lags behind urban construction. Therefore, there are often good building excavation has been building facilities to upgrade the drainage system phenomenon. It brought to the city sewage, and it is clear to the city sewage and drainage culvert in the sewage treatment system. comfort is very important to people's lives. Mobile robots designed to clear the drainage culvert and the automatic control system Free sewage culvert clear guarantee robot, the robot is designed to clear the culvert sewage to the core. Control System is the core component of the development of ultrasonic range finder. Therefore, it is very important to design a good ultrasonic range finder.

2. A principle of ultrasonic distance measurement

2.1 The principle of piezoelectric ultrasonic generator

Piezoelectric ultrasonic generator is the use of piezoelectric crystal resonators to work. Ultrasonic generator, the internal structure as shown, it has two piezoelectric chip and a resonance plate. When it's two plus pulse signal, the frequency equal to the intrinsic piezoelectric oscillation frequency chip, the chip will happen piezoelectric resonance, and promote the development of plate vibration resonance, ultrasound is generated. Conversely, if the two are not inter-electrode voltage, when the board received ultrasonic resonance, it will be for vibration suppression of piezoelectric chip, the mechanical energy is converted to electrical signals, then it becomes the ultrasonic receiver.

The traditional way to determine the moment of the echo's arrival is based on thresholding the received signal with a fixed reference. The threshold is chosen well above the noise level, whereas the moment of arrival of an echo is defined as the first moment the echo signal surpasses that threshold. The intensity of an echo reflecting from an object strongly depends on the object's nature, size and distance from the sensor. Further, the time interval from the echo's starting point to the moment when it surpasses the threshold changes with the intensity of the echo. As a consequence, a considerable error may occur Even two echoes with different intensities arriving exactly at the same time will surpass the threshold at different moments. The stronger one will surpass the threshold earlier than the weaker, so it will be considered as belonging to a nearer object.

2.2The principle of ultrasonic distance measurement

Ultrasonic transmitter in a direction to launch ultrasound, in the moment to launch the beginning of time at the same time, the spread of ultrasound in the air, obstacles on his way to return immediately, the ultrasonic reflected wave received by the receiver immediately stop the clock. Ultrasound in the air as the propagation velocity of 340m / s, according to the timer records the time t, we can calculate the distance between the launch distance barrier (s), that is: s = 340t / 2

3.Ultrasonic Ranging System for the Second Circuit Design

System is characterized by single-chip microcomputer to control the use of ultrasonic transmitter and ultrasonic receiver since the launch from time to time, single-

chip selection of 8751, economic-to-use, and the chip has 4K of ROM, to facilitate programming. Circuit schematic diagram shown in Figure 2.

Figure 1 circuit principle diagram

3.1 40 kHz ultrasonic pulse generated with the launch

Ranging system using the ultrasonic sensor of piezoelectric ceramic sensors UCM40, its operating voltage of the pulse signal is 40kHz, which by the single-chip implementation of the following procedures to generate.

puzel: mov 14h, # 12h; ultrasonic firing continued 200ms

here: cpl p1.0; output 40kHz square wave

Ranging in front of single-chip termination circuit P1.0 input port, single chip implementation of the above procedure, the P1.0 port in a 40kHz pulse output signal, after amplification transistor T, the drive to launch the first ultrasonic UCM40T, issued 40kHz ultrasonic pulse, and the continued launch of 200ms. Ranging the right and the left side of the circuit, respectively, then input port P1.1 and P1.2, the working principle and circuit in front of the same location.

3.2 Reception and processing of ultrasonic

Used to receive the first launch of the first pair UCM40R, the ultrasonic pulse modulation signal into an alternating voltage, the op-amp amplification IC1A and after polarization IC1B to IC2. IC2 is locked loop with audio decoder chip LM567, internal voltage-controlled oscillator center frequency of f0 = 1/1.1R8C3, capacitor C4 determine their target bandwidth. R8-conditioning in the launch of the carrier frequency on the LM567 input signal is greater than 25mV, the output from the high jump 8 feet into a low-level, as interrupt request signals to the single-chip processing.

Ranging in front of single-chip termination circuit output port INT0 interrupt the highest priority, right or left location of the output circuit with output gate IC3A access INT1 port single-chip, while single-chip P1.3 and P1. 4 received input IC3A, interrupted by the process to identify the source of inquiry to deal with, interrupt priority level for the first left right after. Part of the source code is as follows:

receive1: push psw

```
                push acc
                clr ex1; related external interrupt 1
                jnb p1.1, right; P1.1 pin to 0, ranging from right to interrupt
  service routine circuit
                jnb p1.2, left; P1.2 pin to 0, to the left ranging circuit
interrupt
  service routine
  return: SETB EX1; open external interrupt 1
                pop   acc
                pop   psw
                reti
  right: ...;   right location entrance circuit interrupt service routine
                Ajmp  Return
  left: ...;    left Ranging entrance circuit interrupt service routine
                Ajmp  Return
```

3.3 The calculation of ultrasonic propagation time

When you start firing at the same time start the single-chip circuitry within the timer T0, the use of timer counting function records the time and the launch of ultrasonic reflected wave received time. When you receive the ultrasonic reflected wave, the receiver circuit outputs a negative jump in the end of INT0 or INT1 interrupt request generates a signal, single-chip microcomputer in response to external interrupt request, the implementation of the external interrupt service subroutine, read the time difference, calculating the distance . Some of its source code is as follows:

```
  RECEIVE0: PUSH PSW
                PUSH ACC
                CLR EX0; related external interrupt 0
                MOV R7, TH0; read the time value
                MOV R6, TL0
                CLR C
                MOV A, R6
```

```
SUBB A, # 0BBH; calculate the time difference
MOV 31H, A; storage results
MOV A, R7
SUBB A, # 3CH
MOV 30H, A
SETB EX0; open external interrupt 0
POP ACC
POP PSW
RETI
```

For a flat target, a distance measurement consists of two phases: a coarse measurement and. a fine measurement:

Step 1: Transmission of one pulse train to produce a simple ultrasonic wave.

Step 2: Changing the gain of both echo amplifiers according to equation , until the echo is detected.

Step 3: Detection of the amplitudes and zero-crossing times of both echoes.

Step 4: Setting the gains of both echo amplifiers to normalize the output at, say 3 volts. Setting the period of the next pulses according to the : period of echoes. Setting the time window according to the data of step 2.

Step 5: Sending two pulse trains to produce an interfered wave. Testing the zero-crossing times and amplitudes of the echoes. If phase inversion occurs in the echo, determine to otherwise calculate to by interpolation using the amplitudes near the trough. Derive t sub m1 and t sub m2 .

Step 6: Calculation of the distance y using equation .

4. The ultrasonic ranging system software design

Software is divided into two parts, the main program and interrupt service routine. Completion of the work of the main program is initialized, each sequence of ultrasonic transmitting and receiving control.

Interrupt service routines from time to time to complete three of the rotation direction of ultrasonic launch, the main external interrupt service subroutine to read the value of completion time, distance calculation, the results of the output and so on.

5. Conclusions

Required measuring range of 30cm ~ 200cm objects inside the plane to do a number of measurements found that the maximum error is 0.5cm, and good reproducibility. Single-chip design can be seen on the ultrasonic ranging system has a hardware structure is simple, reliable, small features such as measurement error. Therefore, it can be used not only for mobile robot can be used in other detection systems.

Thoughts: As for why the receiver do not have the transistor amplifier circuit, because the magnification well, integrated amplifier, but also with automatic gain control level, magnification to 76dB, the center frequency is 38k to 40k, is exactly resonant ultrasonic sensors frequency.