Electrical Characterization of the Interconnected Mesh Power System (IMPS) MCM Topology

L. W. Schaper, *Member, IEEE,* S. Ang, *Member, IEEE,* Yee L. Low, and Danny R. Oldham

***Abstract*—A significant decrease in MCM substrate production cost can be achieved by reducing the number of substrate layers from the conventional four or five (power, ground, X signal, Y signal, pad) to two or three. Besides reducing direct processing steps, yield will also increase as defect producing operations are eliminated.**

This paper describes the Interconnected Mesh Power System (IMPS), a new interconnection topology which leverages the production technologies of fine line lithography and batch via generation to allow planar power and ground distribution, and dense signal interconnection, on only two metal layers. Several possible implementations of the topology in MCM-D and MCM-L are described.

The design of a test vehicle which characterizes both the signal transmission and power distribution properties of the IMPS topology is discussed. The test vehicle has been built in an aluminum/polyimide on silicon process developed at HiDEC. Results of signal transmission measurements (impedance, delay, and crosstalk) for various signal/power/ground configurations are presented.

Power distribution characteristics (dc drops and ac noise) are presented and compared with measurements on a test vehicle implemented with solid power and ground planes.

From the measured characteristics of the test vehicle, the applicability (clock frequency, power, etc.) for the IMPS topology has been determined. Most MCM applications can benefit from the substrate cost reduction enabled by IMPS.

***Index Terms*—Multichip modules, cost reduction, power distribution, decoupling, interdigitated, mesh planes.**

I. Introduction

BESIDES producing MCM substrates in large panel format to achieve economies of scale, the surest way to achieve substrate cost reduction is to reduce the number of manufacturing process steps. Though material cost reduction and process tweaking can have some impact, more substantial cost reduction can be obtained by eliminating substrate layers. Although some simple MCM's have been made with one or two metal layers, almost all MCM-D implementations have used four or five: power plane, ground plane, X signal, Y signal, and perhaps a pad layer. This topology is a natural extension of printed wiring board construction. Unfortunately for most MCM-D's, every metal layer costs approximately the same, no matter if it is a solid plane or a wiring layer with 300 cm/cm^2 of wiring capability; this is due to deposition and lithography techniques employed. Moreover, the capabilities of batch via production methods have not heretofore been used to advantage in MCM-D and some MCM-L, compared with the sequentially drilled vias of wiring boards.

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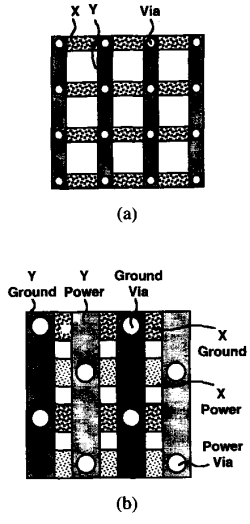

Fig. 1. Derivation of the IMPS topology.

II. The IMPS Topology

The Interconnected Mesh Power System (IMPS) is a new systematic topology which allows low inductance planar power and ground distribution, as well as dense, controlled-impedance, low crosstalk signal transmission in only two physical wiring layers. It utilizes the production methods of fine line lithography and batch via fabrication characteristic of MCM-D and some MCM-L to create a structure not economically possible using standard printed wiring board methods.

The derivation of the power distribution structure is shown sequentially in Fig. 1. Consider a familiar meshed plane, used in many MCM's for power or ground. Think of this construction not as a plane with holes, however, but as a set of X and Y conductors. In Fig. 1(a), the X conductors and Y conductors have been placed on two separate metal layers, and at each crossover, a via has been provided to retain the planar characteristics. (Vias typically have low resistance and inductance compared with lines.) This "interconnected mesh"

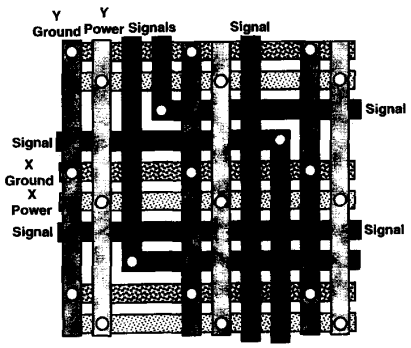

Fig. 2. "Sparse" IMPS implementation.

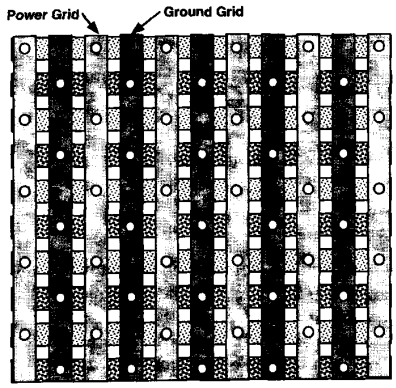

Fig. 3. Coarse mesh.

plane is reasonably electrically equivalent to, but topologically different from, the conventional mesh plane.

The mesh of Fig. 1(a) includes enough space between conductors to insert interdigitated conductors of opposite polarity (power or ground) with their own set of interconnecting vias, on the same two physical metal layers (Fig. 1(b)). The resulting "interconnected mesh" structure forms a complete power distribution system, with the necessary characteristics of low resistance and inductance.

In this "dense" mesh of power and ground conductors, there is no room for signals. Yet if every *other* power and ground conductor (and the corresponding vias) were omitted, the resulting "sparse" power distribution mesh structure would still be planar, but containing less metal, would be more resistive and inductive. Signal wiring at an average spacing twice that of minimum conductor pitch could be provided, as in Fig. 2. However, this arrangement results in adjacent signal tracks, with potentially high crosstalk and poor impedance control.

Many variations of a "fine" (i.e., minimum design rule) interconnected mesh are possible, with signal conductors substituting for up to almost half of the power and ground conductors, but always keeping at least one power or ground conductor between adjacent signal conductors. An ongoing tradeoff between available signal line density and power distribution integrity results, and care must be taken not to "disconnect" portions of a power or ground plane. The following wire sequences indicate several possibilities, with the nP figure denoting average signal line pitch as a multiple of minimum wire pitch:

GSGPGPSPGPGSG....	5P
GSGPSPGSGPSP....	3P
GSGSGPSPSPGS....	2.5P
GSGSGSGSGSGS....	2P NO!

The last sequence could potentially "disconnect" or at least "non-planarize" the power plane.

A better solution is to adopt a "coarse" (i.e., non-minimum design rule) mesh for power distribution. For example, in an MCM-D technology with 20 μm minimum line and space, a design rule of 100 μm line and 60 μm space could be adopted for the power wiring. (Power or ground conductors on 320 μm pitch are shown in Fig. 3.) Signal wiring in areas not requiring very high density would be inserted (20 μm wide

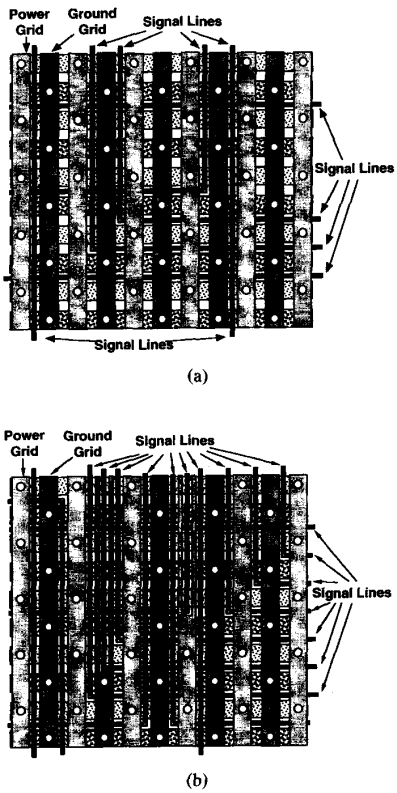

Fig. 4. (a) Signal lines between power and ground. (b) Signal lines at high density.

conductor) into the 60 μm space between power and ground conductors (160 μm signal wire pitch, Fig. 4(a)). In areas where greater signal wire density might be required, signal wires could be "dropped into" power or ground conductors (Fig. 4(b)) with a resulting signal line pitch of 80 μm. Note that the split power or ground conductor uses four signal-sized vias to replace the large power vias at the appropriate crossovers to maintain mesh continuity. The implications of these geometries on signal propagation characteristics will be discussed later. The 80 μm signal line pitch compares well

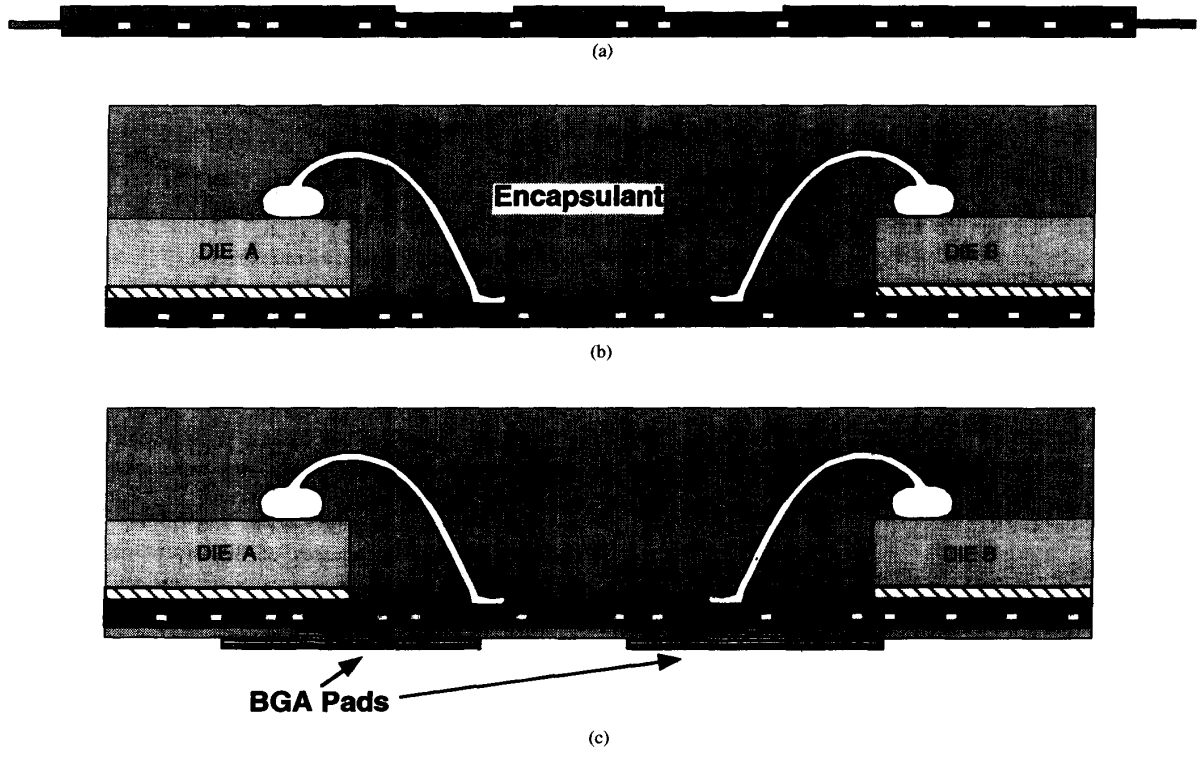

Fig. 5. IMPS on film carrier.

with the 75 μm pitch (25 μm line and 50 μm space) used on many conventional MCM signal layers to reduce crosstalk. The IMPS topology offers far greater crosstalk reduction by interposing an ac ground conductor between every pair of signal conductors.

III. IMPS Topology Implementations

The IMPS topology is easily implemented in a conventional MCM-D process, where fine line lithography and batch fine via fabrication are intrinsic to normal manufacturing. An MCM-L implementation is quite practical, if via fabrication is by other than normal mechanical drilling, and via size is small enough not to impact line pitch.

A two layer process, however, opens up the possibility of fabricating conductors on either side of a piece of polymer film, which could be processed in reel-to-reel format (Fig. 5(a)). The resulting substrate could be populated and tested, then encapsulation applied to form a rigid structure (Fig. 5(b)). Inexpensive screen printing materials and methods could be used to form a ball grid array (BGA) on the bottom of the module, providing a convenient system interface (Fig. 5(c)). Modules of this kind could be extremely inexpensive, yet still yield high performance.

IV. IMPS Analysis and Experiment

Because the IMPS topology is radically different from the conventional microstrip or stripline MCM transmission line environment with solid power and ground planes, a detailed study to determine the characteristics of the power and signal environments was undertaken.

A. Power Distribution

Normal MCM power distribution is by solid metal power and ground planes, sometimes with an intervening thin dielectric which creates a parallel plate decoupling capacitor to supply all, or part, of transient current demands. In most cases, however, surface mounted ceramic capacitors are needed as charge reservoirs to keep transient di/dt noise on these planes below acceptable margins. Conventional chip capacitors have relatively high parasitic inductance and low resonant frequency, however. Special low-inductance capacitors made by AVX, originally designed for the IBM Thermal Conduction Module, provide far better decoupling. The parallel plate P/G planes themselves form a low inductance distribution structure. Wirebonds from these planes to the chips, even though many are paralleled, contribute far more inductance and can critically affect on-chip noise.

The IMPS topology replaces solid planes with a mesh of conductors. In a dual mesh plane of 100 μm wide conductors on 320 μm pitch, net metal coverage is reduced to 62% that of a solid plane. Even with substantial power and ground conductor cuts to accommodate signal wires, metal coverage of 40% can be realized. Increased resistive and inductive parasitics are thus expected. However, since the contribution of these parasitics to dc and ac drops in the solid plane case is

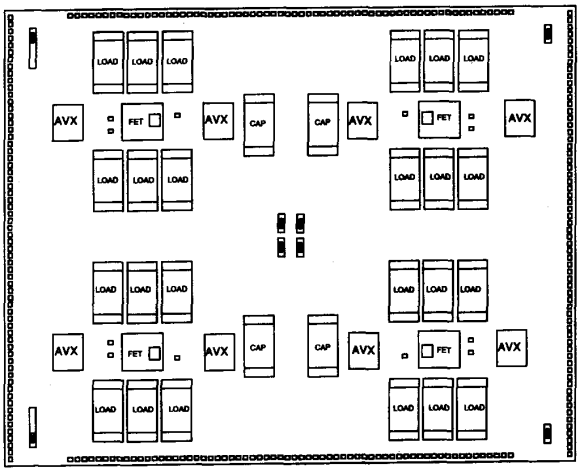

Fig. 6. Test vehicle power transient measurement setup.

often insignificant, this performance decrease is manageable in almost all cases. Attachment of both normal and low-inductance decoupling capacitors in the conventional manner provides the necessary decoupling capacitance over a wide frequency range.

To examine the effectiveness of IMPS power distribution, two test vehicles were designed and built; one with solid planes, the other with IMPS. On each, four n-channel power FET's are arranged to connect on-module resistive loads between power and ground, thus inducing large di/dt into the power distribution structure. As shown in Fig. 6, several sites are provided for normal ceramic, as well as low-inductance chip capacitors. For clarity, other features of the test vehicle, for signal transmission measurements, have not been shown. Various combinations of capacitors and loads, as well as current rise times, were tried. Resulting measurements are described later.

B. Signal Transmission

The IMPS signal transmission environment is shown in Fig. 7. Each signal conductor lies between ac ground conductors on the same metal plane, and over orthogonal power, ground, and signal conductors on the other metal plane. Because the ac ground conductors in the second plane are orthogonal to the signal line of interest, return currents flow only in the coplanar conductors; the orthogonal conductors moderately reduce the line impedance through capacitive loading. This was initially demonstrated by building large-scale physical models (160 times the size of MCM dimensions) and doing TDR measurements, and has been confirmed by measurements on the IMPS test vehicle described below.

C. Test Vehicle

The test vehicle shown in Fig. 8 was designed and fabricated in a HiDEC-developed four mask process using aluminum conductors and photodefinable polyimide dielectric on 5 silicon substrates. The fabrication process began with 2 μm of

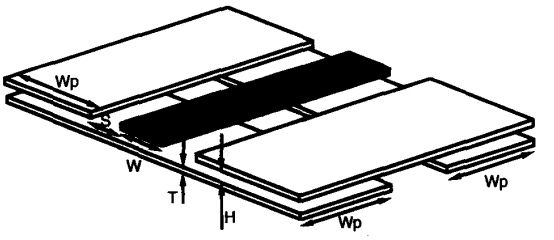

Fig. 7. IMPS signal transmission environment.

SiO_2 deposited by PECVD on bare Si wafers, or an 8 μm layer of DuPont 2721 polyimide. Next 2 μm of Al/1%Si was sputtered and defined by photolithography and wet etching. Next, a layer of polyimide was spun on, exposed, and developed. Mask features of 50 μm for large power vias and 15 μm for signal and small power vias were used. The metal deposition and patterning was repeated to form the second metal layer, and a final polyimide step formed a protective overcoat. Several thicknesses of interlayer and base layer dielectric were compared.

The 33 × 26 mm substrate was populated with decoupling capacitors and terminating resistors and was used, unpackaged, for transmission line and power distribution impedance measurements; or it received power FET chips, decoupling capacitors, and load resistors, and was mounted in a 256 lead CQFP package for measurements of dc drop and ac power distribution noise. The solid plane version used for power distribution measurements was likewise configured. Both substrates were fabricated using the same four masks, with the IMPS substrate occupying six of the eight possible 5 wafer sites, and the solid plane substrate the remaining two sites.

D. Signal Transmission Structures and Measurement Results

Several different signal transmission test structures have been included in the IMPS test vehicle. All have microwave probe pads on 150 μm pitch at either end, and provision to terminate the line using a 50 Ω 0603 size (1.6 × 0.8 mm) chip resistor bonded to the substrate with conductive epoxy. For all transmission line measurements, decoupling capacitors, sufficient to hold the power distribution impedance below 0.5 Ω from 1 MHz to 1 GHz were installed. (See the following section on power distribution impedance.) Second level metal lines either 24.6 mm or 26.6 mm long were configured as signal between power and ground conductors (PSG), signal inside a split power conductor (PSP), and signal inside a split ground conductor (GSG). There is also a crosstalk measurement set of lines, on 80 μm pitch, the driven line lying between power and ground, and the victim line within the adjacent split ground conductor. First level lines (lying on the SiO_2 or polyimide dielectric) 18.2 mm long, configured as PSP, GSG, and PSG were also measured to see if line impedance differed from second metal.

One aspect of the IMPS topology raised particular concern. This was the effect on impedance, and particularly on propagation velocity, of changing from, for example, an X-going

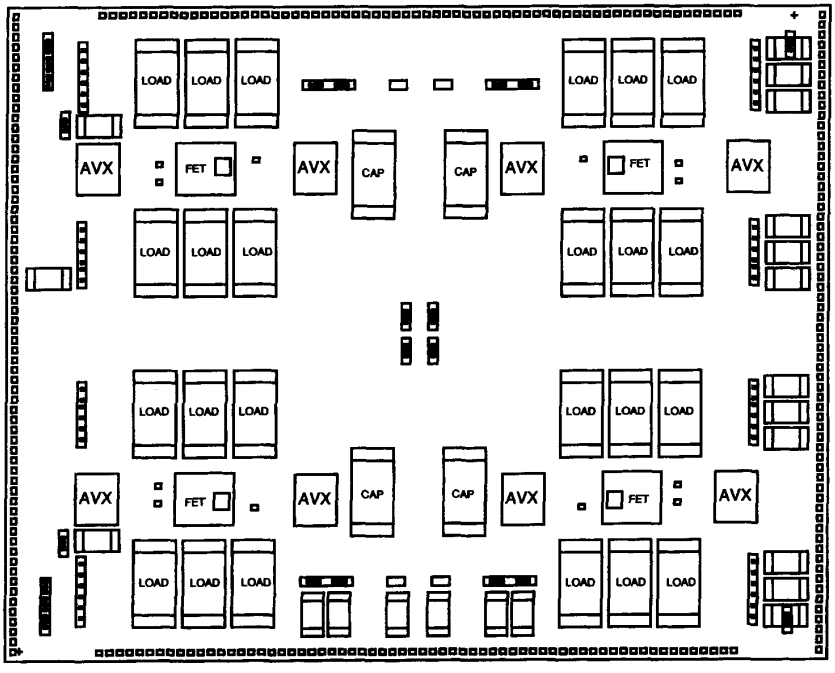

Fig. 8. IMPS test vehicle.

PSP line to a Y-going GSG line. There is a discontinuity at the point of return current path change, which has some effect depending on how well P and G are decoupled at frequencies of interest. This has not appeared to be a problem in many MCM's, where signal layers are routinely referenced either to power or ground planes with no effect. To determine if a problem exists in IMPS, a five segment path was created, with 2.4 mm PSP, 6.3 mm GSG, 11.5 mm PSP, 6.3 mm GSG, and 2.4 mm PSP sections in series.

Substrates with an interlevel and overcoat polyimide thickness of 4.0 μm, and initial SiO_2 dielectric thickness of 2 μm, were built and measured. Measurements were performed using a Tektronix IPA 310 Interconnect Parameter Analyzer. The results are shown below.

	$Z_0\Omega$	t_p ps/cm
M1 PSP	34	90
M1 GSG	34	90
M2 PSP	54	75
M2 GSG	54	75
M2 PSG	54	75
M2 5 Seg	54	75

These measurements indicated a substantial difference between M1 and M2 transmission lines, caused by the thin dielectric layer under M1, and the resulting presence of fields within the partially conducting silicon substrate. The impedance of the M2 lines was higher than expected because a mask error resulted in 16 μm line widths instead of the desired 20 μm. The value of propagation delay determined for M2 is certainly similar to other MCM-D substrates; the M1 figures were higher due to the proximity of the substrate. No problems were caused by signals being referenced to power or ground; the delay of the five segment line was no different from the other M2 lines.

The mask set was revised and the experiment was repeated with 8 μm thick polyimide for the initial dielectric layer, and 5.4 μm of polyimide between M1 and M2. The following results were obtained:

	$Z_0\Omega$	t_p ps/cm
M1 PSP	42	72
M1 GSG	42	72
M1 PSG	42	70
M2 PSP	52	66
M2 GSG	52	66
M2 PSG	52	66
M2 5 Seg	52	68

Even with an 8 μm layer of polyimide, the semiconducting silicon still has an effect. As we are currently using test wafers as substrates, the wafer resistivity is not known. Further fabrication will use measured resistivity wafers to determine the resistivity necessary to eliminate the difference between M1 and M2 transmission lines. Detailed simulations of lines above semiconducting substrates are also in progress. Of course, a different implementation of the topology on an insulating substrate of low dielectric constant would not have this problem.

The crosstalk measurement was made on M2 lines with 28.5 mm coupled length. Both ends of the victim line were terminated. Measurements were made on the IPA 310 by injecting the 20 pS rise time TDR pulse into the driven line and measuring the victim line. Peak crosstalk was less than 3.6% on this set of long coupled lines. This result indicates

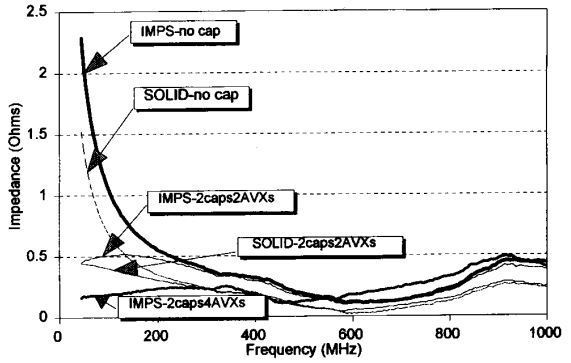

Fig. 9. Power distribution impedance versus frequency using the HP 8510 network analyzer.

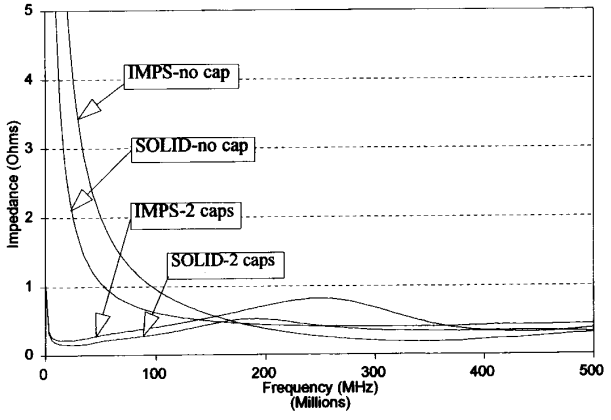

Fig. 10. Power distribution impedance versus frequency using the HP 4291A impedance meter.

that crosstalk should not be a problem at reasonable clock frequencies and line lengths.

E. Power Distribution Impedance Measurements

Power distribution impedance was measured using both an HP 8510 Network Analyzer, and an HP 4291A Impedance Meter. A range of 45 MHz to 1 GHz could be measured with the 8510. Fig. 9 shows the measured impedance for several substrates with various combinations of decoupling capacitance. The effect of even the low inductance AVX capacitors only appears below 300 MHz; above this frequency the intrinsic capacitance of the planes, in either solid (3.2 nF) or IMPS (1.6 nF) versions, dominates the measured impedance. The rising impedance from 600 to 900 MHz is due to inductive effects. With the 4291A, measurements were made from 1 to 500 MHz, as shown in Fig. 10. The resonance of the 0.1 μF chip capacitors is clearly seen around 20 MHz. These measurements were made without AVX capacitors in place in order to confirm the SPICE models, which predict the rise in impedance, with the normal caps in place, between 200 and 300 MHz.

The results indicate that there is little difference between the IMPS power distribution structure and one using solid planes. Any planar effects will be masked by attachment or wirebonding impedances, and by the number and type of capacitors used. The procedure used to attach chip capacitors is extremely important, as the aluminum lines of the substrate form native aluminum oxide rapidly, and even this roughly 80 Å of oxide can produce measurable resistances in power paths. This may account for the inability to achieve extremely low impedances.

F. Power Distribution DC and AC Measurements

The test vehicle shown in Fig. 6 was built in both IMPS and solid plane designs. Each was assembled with two 0.1 μF chip capacitors and four 135 nF AVX capacitors for decoupling. Six paralleled 50 Ω resistors were used as loads (8.3 Ω resistance) for each of the four power FET's. The substrates were assembled into 256 lead CQFP packages with 110 ground and 80 power connections, to ensure solid power distribution to the substrate. These packages were soldered to custom, well decoupled test boards. The resulting assemblies were measured for dc voltage drops with large currents flowing through the load resistors, and for ac noise on the substrate planes with large dI/dt induced by driving the FET gates with a pulse generator.

Because of assembly problems, only three of the four FET load sections could be activated, and some load resistors were inoperative, so the effective resistance of these test vehicles was 3.9 Ω. However, this was sufficiently low that ample current could be drawn, even with the 10 V maximum dictated by decoupling capacitors. The dc drops were measured with 1.9 A total substrate current, and voltage drop was measured between the package wirebond shelf and the center of the substrate, where test points were provided. The total voltage drops were 12 mV for the solid planes and 21 mV for IMPS, for an effective resistance per plane of 3 mΩ for the solid and 5.5 mΩ for IMPS. Based on the amount of metal in the two geometries, this is as expected.

AC noise measurements were made with a total substrate dI/dt of ~0.1 A/ns at the leading edge of the turn-on pulse. Both the solid plane and IMPS versions exhibited peak-to-peak noise voltages of ~200–300 mV, depending on exactly where on the planes the measurements were made. This result, like the measurement of the power distribution impedance, is a reflection of the capacitors and attachment methods more than it is any intrinsic limitation of a planar power distribution structure.

V. Range of IMPS Applications

The IMPS topology can provide, with easily manufactured MCM-D design rules, a variable signal line density up to 250 cm/cm^2 (80 μm pitch on two metal layers), which is comparable with other MCM-D implementations. These are controlled impedance lines which can be tailored to impedances in the 50–70Ω range with appropriate geometries. Because of the intervening ac ground conductor, they exhibit extremely low crosstalk. If greater density were required, selective deletions of power distribution connectivity could be made, or, a four

layer IMPS structure could be produced. This would be a more effective use of metal than the traditional four layer stack.

The loss exhibited by these lines is a function of their material and cross section. Thick (~5–8 μm) plated copper lines would be far less lossy than thin aluminum lines, and are within the process capabilities of several MCM vendors.

The power distribution characteristics of the IMPS compares well with conventional solid planes, both in impedance and noise measurements. Resistive dc drops are expectably greater than with solid planes, but would only be a problem in modules of extremely high power density, and could be reduced to inconsequential levels by thicker plated metal. AC noise is far more affected by wirebond inductance, decoupling capacitor inductance, numbers of capacitors used, and attachment methods, than it is by planar characteristics.

If there are limitations to the IMPS topology, they lie above the frequencies and power densities examined by this test vehicle, and probably above the clock frequencies, line densities, and module powers of interest for near-term high volume applications. Although additional work is needed to refine the measurements presented here, it appears that there is no impediment to adopting this effective cost reduction methodology for most MCM-D applications.

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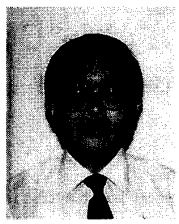
Dr. Schaper has served for many years on the IEPS program committee, as well as on the IEEE Computer Packaging Committee. He is currently a member of the Board of Directors of the IEPS.



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In 1991 he joined HiDEC to study the dielectric properties of diamond MCM substrates. Currently, he is a Ph.D student at the University of Arkansas, and is working on the signal transmission and power distribution properties of the IMPS topology.

Danny R. Oldham received the B.S. degree in electrical engineering at the University of Arkansas in 1992.

He has been responsible for process development of polyimide/aluminum MCM's at HiDEC, as well as the study of the fabrication of IMPS substrates on polyimide film. He is currently working on his M.S. degree.